UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE
United States Patent and Trademark Office
Address: COMMISSIONER FOR PATENTS
P.O. Box 1450
Alexandria, Virginia 22313-1450
www.uspto.gov

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/694,567	10/28/2003	Masatoshi Shinagawa	67471-028	2657

7590 08/25/2005

MCDERMOTT, WILL & EMERY
600 13th Street, N.W.
Washington, DC 20005-3096

EXAMINER	
WASHBURN, DOUGLAS N	

ART UNIT	PAPER NUMBER
2863	

DATE MAILED: 08/25/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/694,567	SHINAGAWA ET AL.	
	Examiner	Art Unit	
	Douglas N. Washburn	2863	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *03 August 2005*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-30* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☒ Claim(s) *28-30* is/are allowed.

6)☒ Claim(s) *1-8,10-13,15,16,18 and 27* is/are rejected.

7)☒ Claim(s) *9,14,17 and 20-26* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *28 October 2003* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Response to Amendment

1 Applicant amendment fails to overcome §102(b) rejection of claims 1-8, 10-13, 15, 16, 18, 19 and 27 and the rejection is maintained.

Claim Rejections - 35 USC § 102

2 The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

Claims 1-8, 10-13, 15, 16, 18, 19 and 27 are rejected under 35 U.S.C. 102(b) as being anticipated by Albertsen (US 5,048,019)(Hereafter referred to as Albertsen).

Albertsen teaches:

A nonvolatile memory (ROM; column 3, line 58; figure1, elements 4 and 6) microcomputer chip comprising a microcomputer unit (CPU; column 3, lines 42 and 43; figure 1, element 1) and a memory unit (program memory 4, ROM 6; column 3, lines 55-60; figure 1, elements 4 and 6), the microcomputer unit including a plurality of circuit blocks including a CPU (e.g.; column 3, lines 41-45; figure 1, elements 1 and 2) in regard to claim 1;

A memory unit including a nonvolatile memory (program memory 4, ROM 6; column 3, lines 55-60; figure 1, elements 4 and 6) in regard to claim 1;

A memory control unit (CPU; column 4, lines 1-7; figure 1, element 2) operable to (a) acquire a plurality of pieces of test data from outside a nonvolatile memory (ROM; column 3, line 58; figure1, elements 4 and 6) microcomputer chip and store a plurality of pieces of test data in a nonvolatile memory (test control circuit; column 4, lines 39-43; figure 1, element 10), and then (b) control the nonvolatile memory (ROM; column 3, line 58; figure1, elements 4 and 6) to sequentially output a plurality of test signals which each show a piece of test data out of the plurality of pieces of test data (test control circuit; column 4, lines 39-43; figure 1, element 10) in regard to claim 1;

A drive unit (switch; column 4, lines 1-7; figure 1, element 8) operable to supply each of a plurality of test signals sequentially output from a nonvolatile memory (ROM; column 3, line 58; figure1, elements 4 and 6), to any of a plurality of circuit blocks that is to be tested using a piece of test data shown by a test signal, to drive the circuit block in regard to claim 1;

An output unit (ALU; column 3, lines 50-54; figure 1, element 12) operable to receive a test result signal from a driven circuit block, and output a test result signal to outside a nonvolatile memory (ROM; column 3, line 58; figure1, elements 4 and 6) microcomputer chip in regard to claim 1;

A port (input/output circuit; column 4, lines 10-12; figure 1, elements 18 and 20) operable to send/receive a signal to/from outside the microcomputer unit, the drive unit (switch; column 4, lines 1-7; figure1, element 8) supplies the test signal to the circuit block through the port (input/output circuit; column 4, lines 10-12; figure 1, elements 18 and 20) and the output unit (ALU; column 3, lines 50-54; figure 1, element 12) receives the test result signal from the circuit block through the port (input/output circuit; column 4, lines 10-12; figure 1, elements 18 and 20) in regard to claim 2;

A memory control unit (CPU; column 4, lines 1-7; figure 1, element 2) (a) acquires a plurality of pieces of expectation data from outside the nonvolatile memory (ROM; column 3, line 58; figure1, elements 4 and 6) microcomputer chip in a one-to-one correspondence with the plurality of pieces of test data, and stores each piece of test data and a corresponding piece of expectation data in a memory area of the nonvolatile memory (ROM; column 3, line 58; figure1, elements 4 and 6) having a unique address, each piece of expectation data representing a test result signal that is expected if a circuit block to which a test signal showing a corresponding piece of test data is output is driven correctly, and then (b) each time an address signal is given from outside the nonvolatile memory (ROM; column 3, line 58; figure1, elements 4 and 6) microcomputer chip, controls the nonvolatile memory (ROM; column 3, line 58; figure1, elements 4 and 6) to output a test signal and an expectation signal that respectively show a piece of test data and a piece of expectation data stored in a memory area having an address shown by the address signal, the drive unit (switch; column 4, lines 1-7; figure1, element 8) supplies the test signal output from the nonvolatile memory (ROM; column 3, line 58; figure1, elements 4 and 6) in response to the address signal, to a circuit block that is to be tested using the piece of test data shown by the test signal, to drive the circuit block, and the output unit (ALU; column 3, lines 50-54; figure 1, element 12) receives a test result signal from the driven circuit block, and outputs the test result signal and the expectation signal together to outside the nonvolatile memory (ROM; column 3, line 58; figure1, elements 4 and 6) microcomputer chip (e.g.; column 4, lines 23-68) in regard to claim 3;

An address generation unit (test control circuit; column 4, lines 58-61; figure 1, element 10) operable to sequentially output a plurality of address signals in regard to claim 4;

A memory control unit (CPU; column 4, lines 1-7; figure1, element 2) (a) stores each piece of test data in a memory area of the nonvolatile memory (ROM; column 3, line 58; figure1, elements 4 and 6) having a unique address, and then (b) each time the address generation unit (test control circuit; column 4, lines 58-61; figure1, element 10) outputs an address signal, controls the nonvolatile memory (ROM; column 3, line 58; figure1, elements 4 and 6) to output a test signal showing a piece of test data stored in a memory area having an address shown by the address signal, and the drive unit (switch; column 4, lines 1-7; figure1, element 8) supplies the test signal output from the nonvolatile memory (ROM; column 3, line 58; figure1, elements 4 and 6) in response to the address signal, to a circuit block that is to be tested using the piece of test data shown by the test signal, to drive the circuit block (column 4, lines 23-68) in regard to claim 4;

A memory control unit (CPU; column 4, lines 1-7; figure1, element 2) (a) acquires a plurality of pieces of control data from outside the nonvolatile memory (ROM; column 3, line 58; figure1, elements 4 and 6) microcomputer chip in a one-to-one correspondence with the plurality of pieces of test data (column 4, lines 23-27), and stores each piece of control data in a memory area of the nonvolatile memory (ROM; column 3, line 58; figure1, elements 4 and 6) in which a corresponding piece of test data is stored (column 4, lines 39-43), the plurality of pieces of control data designating an order in which the plurality of pieces of test data are used (column 4, lines 58-66), and then (b) each time the address generation unit (test control circuit; column 4, lines 58-61; figure 1, element 10) outputs an address signal, controls the nonvolatile memory (ROM; column 3, line 58; figure1, elements 4 and 6) to output a test signal and a control signal which respectively show a piece of test data and a piece of control data stored in a memory area having an address shown by the address signal, and the address generation unit (test control circuit; column 4, lines 58-61; figure1, element 10) includes: a counter unit holding a count value, and operable to periodically output an address signal showing the count value and increment the count value by 1, and a counter control unit operable to (i) store the count value held by the counter unit when the nonvolatile memory (ROM; column 3, line 58; figure1, elements 4 and 6) outputs a control signal showing a piece of control data having a first value, and subsequently (ii) replaces the count value held by the counter unit with the stored count value when the nonvolatile memory (ROM; column 3, line 58; figure1, elements 4 and 6) outputs a control signal showing a piece of control data having a second value (column 4, lines 66 et seq; column 5, lines 1-6) in regard to claim 5;

A plurality of pieces of test data (word; column 4, lines 39-43) are divided into test data groups, with a piece of test data at the end of each test data group being end data that can be distinguished from other pieces of test data, and the address generation unit (test control circuit; column 4, lines 58-61; figure 1, element 10) includes: an address storage unit (register; column 4, line 42; figure 1, element 14) operable to store an address of a memory area of the nonvolatile memory (ROM; column 3, line 58; figure1, elements 4 and 6) in which a piece of test data at the beginning of each test data group is stored, a counter unit holding a count value (test control circuit; column 4, lines 39-43; figure 1, element 10), and operable to periodically output an address signal showing the count value and increment the count value by 1 (test control circuit; column 4, lines 58-66; figure 1, element 10), and a counter control unit operable to replace the count value held by the counter unit with one of addresses stored in the address storage unit, when the nonvolatile memory (ROM; column 3, line 58; figure1, elements 4 and 6) outputs a test signal showing the end data (test control circuit; column 4, lines 58-62; figure 1, element 10) in regard to claim 6;

A plurality of pieces of test data (word; column 4, lines 39-43) are divided into test data groups, with a piece of test data at the end of each test data group being end data that can be distinguished from other pieces of test data, the address generation unit (test control circuit; column 4, lines 58-61; figure 1, element 10) includes: an address storage unit (register; column 4, line 42; figure 1, element 14) operable to acquire a plurality of addresses and a plurality of control flag values which are in a one-to-one correspondence with each other from outside the nonvolatile memory (ROM; column 3, line 58; figure1, elements 4 and 6) microcomputer chip, and store the plurality of addresses and the plurality of control flag values beforehand (column 5, lines 29-36), and a release signal acquisition unit (test control circuit; column 5, lines 7-16; figure 1, element 10) operable to acquire a release signal from outside the nonvolatile memory (ROM; column 3, line 58; figure1, elements 4 and 6) microcomputer chip, and the address generation unit (test control circuit; column 4, lines 58-66; figure 1, element 10), for each address stored in the address storage unit, (1) outputs an address signal showing the address, (2) if a corresponding control flag value is a first value, subsequently outputs address signals which show consecutive addresses following the address in sequence, until the nonvolatile memory (ROM; column 3, line 58; figure1, elements 4 and 6) outputs a test signal showing the end data, and (3) if the corresponding control flag value is a second value, subsequently outputs address signals which uniformly show the address in sequence, until the release signal acquisition unit (test control circuit; column 5, lines 7-13; figure 1, element 10) acquires the release signal in regard to claim 7;

A memory control unit (CPU; column 4, lines 1-7; figure1, element 2) includes an address adjustment unit operable to: (1) hold a repetition start address, a repetition end address, and a repetition number, (2) sequentially receive a plurality of address signals, and (3) each time an address signal is received, (i) output the address signal if an address shown by the address signal is different from the repetition start address, and (ii) repeat, a number of times equivalent to the repetition number, outputting address signals which show consecutive addresses from the repetition start address to the repetition end address in sequence, if the address shown by the address signal is same as the repetition start address, the memory control unit (CPU; column 4, lines 1-7; figure1, element 2) (a) stores each piece of test data in a memory area of the nonvolatile memory (ROM; column 3, line 58; figure1, elements 4 and 6) having a unique address, and then (b) each time the address adjustment unit outputs an address signal, controls the nonvolatile memory (ROM; column 3, line 58; figure1, elements 4 and 6) to output a test signal showing a piece of test data stored in a memory area having an address shown by the address signal, and the drive unit (switch; column 4, lines 1-7; figure1, element 8) supplies the test signal output from the nonvolatile memory (ROM; column 3, line 58; figure1, elements 4 and 6) in response to the address signal, to a circuit block that is to be tested using the piece of test data shown by the test signal, to drive the circuit block (column 4, lines 23-68) in regard to claim 8;

A drive unit (switch; column 4, lines 1-7; figure1, element 8) shifts a test signal in level based on an input signal reference voltage applied from outside a nonvolatile memory (ROM; column 3, line 58; figure1, elements 4 and 6) microcomputer chip, and supplies the shifted test signal to a circuit block to drive the circuit block, and an output unit (ALU; column 3, lines 50-54; figure 1, element 12) shifts a test result signal in level based on a comparison reference voltage applied from outside the nonvolatile memory (ROM; column 3, line 58; figure1, elements 4 and 6) microcomputer chip, and outputs the shifted test result signal to outside the nonvolatile memory (ROM; column 3, line 58; figure1, elements 4 and 6) microcomputer chip (column 4, lines 23-68) in regard to claim 10;

A plurality of pairs of connection lines which are provided in a one-to-one correspondence with the plurality of circuit blocks, and each operable to transfer a signal between a corresponding circuit block and the drive unit (switch; column 4, lines 1-7; figure1, element 8) and between the corresponding circuit block and the output unit (ALU; column 3, lines 50-54; figure 1, element 12), the drive unit (switch; column 4, lines 1-7; figure1, element 8) supplies the test signal to the circuit block through one connection line out of a pair of connection lines corresponding to the circuit block, and the output unit (ALU; column 3, lines 50-54; figure 1, element 12) receives the test result signal from the circuit block through the other connection line out of the pair of connection lines corresponding to the circuit block (column 4, lines 1-4) in regard to claim 11;

A memory control unit (CPU; column 4, lines 1-7; figure1, element 2) (a) stores each piece of test data in a memory area of the nonvolatile memory (ROM; column 3, line 58; figure1, elements 4 and 6) having a unique address, and then (b) each time an address signal is given from outside the nonvolatile memory (ROM; column 3, line 58; figure1, elements 4 and 6) microcomputer chip, controls the nonvolatile memory (ROM; column 3, line 58; figure1, elements 4 and 6) to output a test signal showing a piece of test data stored in a memory area having an address shown by the address signal, the memory unit further includes: a circuit block specification unit operable to specify a circuit block that is to be tested using the piece of test data shown by the test signal output from the nonvolatile memory (ROM; column 3, line 58; figure1, elements 4 and 6) in response to the address signal, based on the address signal, and the drive unit (switch; column 4, lines 1-7; figure1, element 8) supplies the test signal to the circuit block specified by the circuit block specification unit, to drive the circuit block (column 4, lines 23-68) in regard to claim 12;

A memory control unit (CPU; column 4, lines 1-7; figure1, element 2) (a) acquires a plurality of pieces of selection data from outside the nonvolatile memory (ROM; column 3, line 58; figure1, elements 4 and 6) microcomputer chip in a one-to-one correspondence with the plurality of pieces of test data, and stores each piece of test data and a corresponding piece of selection data in a memory area of the nonvolatile memory (ROM; column 3, line 58; figure1, elements 4 and 6) having a unique address, each piece of selection data being used for specifying a circuit block that is to be tested using a corresponding piece of test data, and then (b) each time an address signal is given from outside the nonvolatile memory (ROM; column 3, line 58; figure1, elements 4 and 6) microcomputer chip, controls the nonvolatile memory (ROM; column 3, line 58; figure1, elements 4 and 6) to output a test signal and a selection signal which respectively show a piece of test data and a piece of selection data stored in a memory area having an address shown by the address signal, and the drive unit (switch; column 4, lines 1-7; figure1, element 8) supplies the test signal output from the nonvolatile memory (ROM; column 3, line 58; figure1, elements 4 and 6) in response to the address signal, to a circuit block that is specified according to the selection signal, to drive the circuit block (column 4, lines 23-68) in regard to claim 13;

A nonvolatile memory (ROM; column 3, line 58; figure1, elements 4 and 6) includes an oscillation circuit operable to generate a first clock signal, and the nonvolatile memory (ROM; column 3, line 58; figure1, elements 4 and 6) microcomputer chip further comprises a selection circuit operable to selectively supply one of the first clock signal and a second clock signal which is fed from outside the nonvolatile memory (ROM; column 3, line 58; figure1, elements 4 and 6) microcomputer chip, to each circuit block in the microcomputer unit (column 4, lines 23-68) in regard to claim 15;

A memory control unit (CPU; column 4, lines 1-7; figure1, element 2) (a) acquires a plurality of pieces of selection data from outside the nonvolatile memory (ROM; column 3, line 58; figure1, elements 4 and 6) microcomputer chip in a one-to-one correspondence with the plurality of pieces of test data, and stores each piece of test data and a corresponding piece of selection data in a memory area of the nonvolatile memory (ROM; column 3, line 58; figure1, elements 4 and 6) having a unique address, each piece of selection data being used for selecting one of the first clock signal and the second clock signal, and then (b) each time an address signal is given from outside the nonvolatile memory (ROM; column 3, line 58; figure1, elements 4 and 6) microcomputer chip, controls the nonvolatile memory (ROM; column 3, line 58; figure1, elements 4 and 6) to output a test signal and a selection signal which respectively show a piece of test data and a piece of selection data stored in a memory area having an address shown by the address signal, and the selection circuit supplies one of the first clock signal and the second clock signal that is selected according to the selection signal, to each circuit block in the microcomputer unit (column 4, lines 23-68) in regard to claim 16;

A memory control unit (CPU; column 4, lines 1-7; figure1, element 2) (a) acquires a plurality of pieces of selection data from outside the nonvolatile memory (ROM; column 3, line 58; figure1, elements 4 and 6) microcomputer chip in a one-to-one correspondence with the plurality of pieces of test data, and stores each piece of test data and a corresponding piece of selection data in a memory area of the nonvolatile memory (ROM; column 3, line 58; figure1, elements 4 and 6) having a unique address, each piece of selection data being used for selecting a delay time, and then (b) each time an address signal is given from outside the nonvolatile memory (ROM; column 3, line 58; figure1, elements 4 and 6) microcomputer chip, controls the nonvolatile memory (ROM; column 3, line 58; figure1, elements 4 and 6) to output a test signal and a selection signal which respectively show a piece of test data and apiece of selection data stored in a memory area having 16 an address shown by the address signal, the output unit (ALU; column 3, lines 50-54; figure 1, element 12) includes: a delay unit operable to delay a test result signal received from a circuit block which is driven by the test signal output from the nonvolatile memory (ROM; column 3, line 58; figure1, elements 4 and 6) in response to the address signal, by a delay time that is selected from a plurality of predetermined delay times according to the selection signal, and the output unit (ALU; column 3, lines 50-54; figure 1, element 12) outputs the delayed test result signal to outside the nonvolatile memory (ROM; column 3, line 58; figure1, elements 4 and 6) microcomputer chip (column 5, lines 21-63) in regard to claim 18;

A memory control unit (CPU; column 4, lines 1-7; figure1, element 2) (a) acquires a plurality of pieces of selection data from outside the nonvolatile memory (ROM; column 3, line 58; figure1, elements 4 and 6) microcomputer chip in a one-to-one correspondence with the plurality of pieces of test data, and stores each piece of test data and a corresponding piece of selection data in a memory area of the nonvolatile memory (ROM; column 3, line 58; figure1, elements 4 and 6) having a unique address, each piece of selection data being used for selecting a delay time, and then (b) each time an address signal is given from outside the nonvolatile memory (ROM; column 3, line 58; figure1, elements 4 and 6) microcomputer chip, controls the nonvolatile memory (ROM; column 3, line 58; figure1, elements 4 and 6) to output a test signal and a selection signal which respectively show a piece of test data and apiece of selection data stored in a memory area having 16 an address shown by the address signal, the drive unit (switch; column 4, lines 1-7; figure1, element 8) includes: a delay unit operable to delay the test signal output from the nonvolatile memory (ROM; column 3, line 58; figure1, elements 4 and 6) in response to the address signal, by a delay time that is selected from a plurality of predetermined delay times according to the selection signal, and the drive unit (switch; column 4, lines 1-7; figure1, element 8) supplies the delayed test signal to a circuit block that is to be tested using the piece of test data shown by the delayed test signal, to drive the circuit block (column 5, lines 21-63) in regard to claim 19;

And a memory control unit (CPU; column 4, lines 1-7; figure1, element 2) supplies a data signal showing a non-operation instruction, to the CPU, and the CPU executes the non-operation instruction shown by the data signal a plurality of times to sequentially output address signals which show consecutive addresses (column 4, lines 23-68), thereby serving as the address generation unit (test control circuit; column 4, lines 58-61; figure1, element 10) in regard to claim 27.

Allowable Subject Matter

3 Claims 28-30 previously indicated allowable.

Claims 9, 14, 17 and 20-26 are objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

The following is an examiner's statement of reasons for allowance:

Claim 9 recites, in part, "the drive unit supplies a mixed signal to the port, the mixed signal being made up of a test signal showing a piece of test data whose bit length is not largest among the plurality of pieces of test data and one part of an expectation signal output from the nonvolatile memory together with the test signal". This feature in combination with the remaining claimed structure avoids the prior art of record.

Claim 14 recites, in part, "wherein if two nonvolatile memories out of the plurality of nonvolatile memories are to output test signals showing pieces of test data used for testing a same circuit block, the memory control unit allows one of the two nonvolatile memories to output a test signal and prohibits the other nonvolatile memory from outputting a test signal". This feature in combination with the remaining claimed structure avoids the prior art of record.

Claim 17 recites, in part, "the memory control unit (a) acquires a plurality of pieces of selection data from outside the nonvolatile memory microcomputer chip in a one-to-one correspondence with the plurality of pieces of test data, and stores each piece of test data and a corresponding piece of selection data in a memory area of the nonvolatile memory having a unique address, each piece of selection data being used for selecting a frequency of the first clock signal". This feature in combination with the remaining claimed structure avoids the prior art of record.

Claim 20 recites, in part, "the memory control unit (a) acquires a plurality of pieces of designation data from outside the nonvolatile memory microcomputer chip in a one-to-one correspondence with the plurality of pieces of test data, and stores each piece of test data and a corresponding piece of designation data in a memory area of the nonvolatile memory having a unique address, each piece of designation data being used for designating a voltage". This feature in combination with the remaining claimed structure avoids the prior art of record.

Claim 21 recites, in part, "a D/A conversion circuit which serves as the power supply unit, wherein the D/A conversion circuit generates the internal power by digital-to-analog converting the piece of designation data shown by the designation signal, and supplies the internal power to the circuit block as the operating power". This feature in combination with the remaining claimed structure avoids the prior art of record.

Claim 22 recites, in part, "a voltage adjustment circuit operable to generate the internal power by stepping-down the stepped-up voltage of the external power to the voltage designated according to the designation signal, and supply the internal power to the circuit block as the operating power". This feature in combination with the remaining claimed structure avoids the prior art of record.

Claim 23 recites, in part, "a current judgment unit operable to judge whether a power supply current applied to the microcomputer unit exceeds a current designated according to the designation signal, and output a current judgment signal showing a result of the judgment". This feature in combination with the remaining claimed structure avoids the prior art of record.

Claim 24 recites, in part, "a sense amplifier through which the power supply current passes, and which serves as the current judgment unit, wherein the sense amplifier generates a reference current according to the designation signal, and outputs the current judgment signal based on a comparison between the reference current and the power supply current". This feature in combination with the remaining claimed structure avoids the prior art of record.

Claim 25 recites, in part, "when a defective signal is given from outside the nonvolatile memory microcomputer chip in response to the test result signal and the expectation signal, the memory control unit stores the address shown by the address signal to a predetermined memory area of the nonvolatile memory, the defective signal indicating that the circuit block is judged as being defective as a result of testing". This feature in combination with the remaining claimed structure avoids the prior art of record.

Claim 26 recites, in part, "the memory control unit (b) when the defective signal is given from outside the nonvolatile memory microcomputer chip, stores the address shown by the address signal to the predetermined memory area of the nonvolatile memory, and subsequently supplies a control signal to the CPU, the control signal instructing to execute the program from an address of a memory area storing a beginning instruction". This feature in combination with the remaining claimed structure avoids the prior art of record.

It is these limitations, which are not found, taught or suggested in the prior art of record, and are recited in the claimed combination that makes these claims allowable over the prior art.

Response to Arguments

4 Applicant's arguments filed 3 August 2005 have been fully considered but they are not persuasive. Applicant's argument "the same memory can be used during both testing and normal operation so that a separate memory for storing test data is not necessary." is not claimed. Albertsen teaches "a program memory 4 which contains the program to be executed by the microcontroller during normal operation and which is constructed as a read-only memory (ROM), as well as a further read-only memory 6 which contains the test program" (column 3, lines 55-60) read on the broad limitation of claim 1 "a nonvolatile memory operable to store therein test data used for testing when the testing is performed, and operation data used for an operation other than the testing when the operation is performed" therefore the rejection is maintained.

Conclusion

5 **THIS ACTION IS MADE FINAL.** Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the mailing date of this final action.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Douglas N. Washburn whose telephone number is (571) 272-2284. The examiner can normally be reached on Monday through Thursday 6:30 AM - 4:30 PM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, John E. Barlow can be reached on (571) 272-2269. The fax phone number for the organization where this application or proceeding is assigned is 571 273 8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR.

Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

DNW

BRYAN BUI
PRIMARY EXAMINER